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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/538,684	03/30/00	KINSMAN	L 3056.1US (96

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EXAMINER	
GRAYBILL,D	
ART UNIT	**PAPER NUMBER**
2814	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application 09/538,684	Applicant(s) KINSMAN ET AL.	
	Examiner David E Graybill	Art Unit 2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 February 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-45* is/are pending in the application.

4a) Of the above claim(s) *7,21,23 and 32* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,8-20,22,24-31 and 33-45* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

15) ☒ Notice of References Cited (PTO-892)
16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
17) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2* .
18) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
19) ☐ Notice of Informal Patent Application (PTO-152)
20) ☐ Other: .

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 2-4 and 27-29 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claims 2-4 and 27-29 the language, "a group comprising" is improper Markush language.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2, 4-6, 8-20, 24-27, 29-31 and 33-45 are rejected under 35 U.S.C. 102(e) as being anticipated by Marrs (5701034).

Reference labels are recited only for the first recitation of identical claim language.

At column 1, lines 37-44; column 2, lines 33-42; column 3, lines 34-40; column 5, lines 1-33; column 6, lines 19-23 and 59-61; column 8, lines 63 and 64; column 10, lines 17, 18, 24 and

42-46; and column 11, lines 35 and 36, Marrs teaches the following:

1. An integrated circuit (IC) package comprising: a package body 120; an IC die 101 positioned within the package body; a lead frame including a plurality of leads 102 having portions enclosed within the package body that connect to the IC die; and an electrically conductive heat sink 110 positioned at least partially within the package body with a surface 110b of a first portion of the heat sink facing the lead frame in close proximity to a substantial part of the enclosed portion of each of the plurality of leads of the lead frame and with a die-attach area on the surface of the first portion of the heat sink attached to the IC die, a second portion of the heat sink 110a projecting away from the first portion of the heat sink under the die-attach area and the IC die

2. The IC package of claim 1, wherein the package body is selected from a group comprising a transfer molded plastic package body and a preformed ceramic package body.

4. The IC package of claim 1, wherein the lead frame is selected from a group comprising a peripheral-lead finger lead frame, a Leads Over Chip (LOC) lead frame, and a Leads Under Chip (LUC) lead frame.

5. The IC package of claim 1, wherein the heat sink is coupled to one of a signal voltage 206 and a reference voltage so the heat sink operates respectively as a signal plane and a ground plane for the plurality of leads of the lead frame.

6. The IC package of claim 5, wherein the heat sink is coupled to the reference voltage through one of a wirebond 117, a conductive adhesive, and a welded connection.

8. The IC package of claim 1, wherein the heat sink is positioned only partially within the package body (surface 110a is externally exposed).

9. The IC package of claim 1, wherein the heat sink is coupled to a printed circuit board outside the package body and is thereby coupled (by leads 102) to one of a signal voltage and a reference voltage so the heat sink operates respectively as a signal plane and a ground plane for the plurality of leads of the lead frame.

10. The IC package of claim 8, wherein the second portion of the heat sink projects substantially to one of a top and a bottom of the package body.

11. The IC package of claim 1, wherein the heat sink is positioned within the package body with the surface of its first portion in close proximity to substantially all of the enclosed portion of each of the plurality of leads of the lead frame.

12. The IC package of claim 1, wherein the heat sink is positioned within the package body with its first portion extending i substantially to at least one side of the package body.

13. The IC package of claim 1, wherein the heat sink is positioned within the package body with the surface of its first portion in close proximity to at least eighty percent of an area of the enclosed portions of the plurality of leads of the lead frame.

14. The IC package of claim 1, wherein the first and second portions of the heat sink are integral with one another.

15. The IC package of claim 1, wherein the first and second portions of the heat sink comprise separate parts.

16. The IC package of claim 1, wherein the heat sink comprises a plurality of parts, each forming a portion of both the first and second portions of the heat sink.

17. The IC package of claim 1, wherein the surface of the first portion of the heat sink includes a recess in which the die-attach area is located.

18. The IC package of claim 1, wherein the heat sink has locking holes 112 therein for locking the heat sink in the IC package.

19. The IC package of claim 1, further comprising an adhesive 118 attaching the lead frame to the heat sink.

20. The IC package of claim 1, wherein the IC package comprises one of a Vertical Surface Mount Package (VSMP), a Small Outline J-lead (SOJ) package, a Thin Small Outline Package (TSOP), a Quad Flat Pack (QFP), and a Thin QFP (TQFP).

24. An integrated circuit (IC) package comprising: a package body; an IC die positioned within the package body; a lead frame including a plurality of leads having portions enclosed within the package body that connect to the IC die; and

an electrically conductive heat sink positioned at least partially within the package body with a vertically extending columnar portion surrounded by a horizontally extending skirt portion (rim/periphery/edge) having a lead frame attachment surface proximate a die-attach surface substantially vertically aligned with the columnar portion, the lead frame attachment surface being attached to the lead frame and extending in close proximity to a substantial part of the enclosed portions of the plurality of leads of the lead frame, the die-attach surface being attached to the IC die.

25. An integrated circuit (IC) package comprising: an IC die; a lead frame including a plurality of leads having portions that are connected to the IC die; and an electrically conductive heat sink positioned having a surface of a first portion of the heat sink facing the lead frame in close proximity to a substantial

part of an enclosed portion of each of the plurality of leads of the lead frame and with a die-attach area on the surface of the first portion of the heat sink attached to the IC die, a second portion of the heat sink projecting away from the first portion of the heat sink under the die-attach area and the IC die.

26. The IC package of claim 25, further comprising a package body.

27. The IC package of claim 26, wherein the package body is selected from a group comprising a transfer molded plastic package body and a preformed ceramic package body.

29. The IC package of claim 25, wherein the lead frame is selected from a group comprising a peripheral-lead finger lead frame, a Leads Over Chip (LOC) lead frame, and a Leads Under Chip (LUC) lead frame.

30. The IC package of claim 25, wherein the heat sink is coupled to one of a signal voltage and a reference voltage so the heat sink operates respectively as a signal plane and a ground plane for the plurality of leads of the lead frame.

31. The IC package of claim 30, wherein the heat sink is coupled to the reference voltage through one of a wirebond, a conductive adhesive, and a welded connection.

33. The IC package of claim 26, wherein the heat sink is positioned only partially within the package body.

34. The IC package of claim 26, wherein the heat sink is coupled to a printed circuit board outside the package body and is thereby coupled to one of a signal voltage and a reference voltage so the heat sink operates respectively as a signal plane and a ground plane for the plurality of leads of the lead frame.

35. The IC package of claim 34, wherein the second portion of the heat sink projects substantially to one of a top and a bottom of the package body.

36. The IC package of claim 26, wherein the heat sink is positioned within the package body with the surface of its first portion in close proximity to substantially all of the enclosed portion of each of the plurality of leads of the lead frame.

37. The IC package of claim 26, wherein the heat sink is positioned within the package body with its first portion extending substantially to at least one side of the package body.

38. The IC package of claim 26, wherein the heat sink is positioned within the package body with the surface of its first portion in close proximity to at least eighty percent of an area of the lead frame.

39. The IC package of claim 25, wherein the first and second portions of the heat sink are integral with one another.

40. The IC package of claim 25, wherein the first and second portions of the heat sink comprise separate parts.

41. The IC package of claim 25, wherein the heat sink comprises a plurality of parts, each forming a portion of both the first and second portions of the heat sink.

42. The IC package of claim 25, wherein the surface of the first portion of the heat sink includes a recess in which the die-attach area is located.

43. The IC package of claim 25, wherein the heat sink has locking holes therein for locking the heat sink in the IC package.

44. The IC package of claim 25, further comprising an adhesive attaching the lead frame to the heat sink.

45. The IC package of claim 25, wherein the IC package comprises one of a Vertical Surface Mount Package (VSMP), a Small Outline J-lead (SOJ) package, a Thin Small Outline Package (TSOP), a Quad Flat Pack (QFP), and a Thin QFP (TQFP).

Claims 3, 22 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Marrs as applied to claims 1, 2, 4-6, 8-20, 24-27, 29-31 and 33-45, and further in combination with Wark (5696031).

Marrs does not appear to explicitly teach the following:

3. The IC package of claim 1, wherein the IC die is selected from a group comprising a Dynamic Random Access Memory (DRAM) IC die, a Static Random Access Memory (SRAM) IC die, a Synchronous DRAM (SDRAM) IC die, a Sequential Graphics Random Access Memory (SGRAM) IC die, a flash Electrically Erasable Programmable ReadOnly Memory (EEPROM) IC die, and a processor IC die.

22. An electronic system comprising an input device, an output device, a memory device, and a processor device coupled to the input, output, and memory devices, at least one of the input, output, memory, and processor devices including an integrated circuit (IC) package comprising: a package body; an IC die positioned within the package body; a lead frame including a plurality of leads having portions enclosed within the package body that connect to the IC die; and an electrically conductive heat sink positioned at least partially within the package body with a surface of a first portion of the heat sink facing the lead frame in close proximity to a substantial part of the enclosed portion of each of the plurality of leads of the lead frame and having a die-attach area on the surface of the first portion of the heat sink attached to the IC die, a second portion of the heat sink being opposite the die-attach area and projecting away from the first portion of the heat sink and the IC die.

28. The IC package of claim 25, wherein the IC die is selected from a group comprising a Dynamic Random Access Memory (DRAM) IC die, a Static Random Access Memory (SRAM) IC die, a Synchronous DRAM (SDRAM) IC die, a Sequential Graphics Random Access Memory (SGRAM) IC die, a flash Electrically Erasable Programmable ReadOnly Memory (EEPROM) IC die, and a processor IC die.

Nonetheless, at column 5, lines 59-65, Wark teaches these limitations. Moreover, it would have been obvious to combine the product of Wark with the product of Marrs because it would provide an electronic system.

Any telephone inquiry of a general nature or relating to the status (MPEP 203.08) of this application or proceeding should be directed to the group receptionist whose telephone number is 703-308-1782.

Any telephone inquiry concerning this communication or earlier communications from the examiner should be directed to David E. Graybill at (703) 308-2947. Regular office hours: Monday through Friday, 8:30 a.m. to 6:00 p.m.

The fax phone number for group 2800 is 703/305-3431.

David E. Graybill
Primary Examiner
Art Unit 2814

D.G.
16-Mar-01